§ 102(e) as being anticipated by Jeng. (U.S. Patent No. 6,054,769). Claims 2, 6, 31-33 and 38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeng ('769) in view of the applicant's admitted prior art. Claims 39 and 40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jeng ('769) in view of Allada, et al. (U.S. Patent No. 6,218, 317 B1). Reconsideration is respectfully requested.

These rejections are respectfully traversed in view of the following discussion.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Attached hereto is a marked-up version of the changes made to the specification and/or claims by the current Amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example, by independent claim 1, is directed to a semiconductor device having a multi-layered insulation film which includes a first insulation layer having an organic material with a dielectric constant which is lower than a silicon oxide dielectric constant, a second insulation layer including a polysiloxane compound having an Si-H group and formed on and adhering to a top of the first insulation layer, a third insulation layer comprising an inorganic material and formed on and adhering to

a top of the second insulation layer, and a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. (See Page 21, lines 1-21; and Figures 1 and 4).

Conventional devices have a first layer composed of an organic material of low dielectric, i.e., an organic SOG film e.g., Methyl Silsesquioxane ("MSQ") coated with a layer composed of an inorganic protective film, e.g., silicon oxide film. However, the conventional art is not effective because peeling occurs at the interface of the inorganic protective film and the organic layer, and thus de-lamination due to insufficent adhesion produces cross-talk in the semiconductor device . (See Page 2, lines 12-27; and Page 6, line 23 - Page 2, line 4).

An aspect of the present invention includes a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of the first insulation layer as well as a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. This second layer provides excellent interlayer adhesion to the first insulation layer as well as with the third insulation layer while having insulative characteristics. (See Page 6, lines 15-20; Page 16, lines 14-21).

As a result of this inventive structure, the interfacial adhesion between the film with low dielectric constant, i.e., the first insulation layer, and protective film, i.e., the second insulation, adhesive layer, is significantly improved, "without damaging the excellent dielectric, flatness and gap-filling characteristics of the organic material of the low dielectric constant." (See Page 6, lines 15-20).

II. THE 35 U.S.C. § 112, FIRST AND SECOND PARAGRAPH REJECTIONS

Applicant respectfully traverses the 35, U.S.C. § 112, rejection to claim 35. Claim 35

contains subject matter which was described in the specification in such a way to enable one skilled in the art to make and/or use the invention. In particular, the specification explicitly indicates that, "[T]he multi-layered insulation film for the present invention may have another layer of, e.g., MSQ, placed in the second insulation layer." (See Specification, Page 17, lines 15-17). Thus, the second insulation layer may include a first layer and a second layer placed in the first layer as recited in claim 35.

Further, Applicant has amended claim 36 to depend from claim 1 and respectfully submits that the above amended claim 36 particularly points and distinctly claims the subject matter of the invention, and thus fulfills the requirements of 35 U.S.C. § 112, second paragraph.

In view of the foregoing, the Examiner is respectfully requested to withdraw these rejections.

III. THE PRIOR ART REJECTIONS

A. The 35 USC § 102(e) Rejection Based on Jeng

Applicant submits that there are elements of the claimed invention which are neither taught nor suggested by Jeng. Jeng fails to teach or suggest a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. Jeng also fails to teach or suggest a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of the first insulation layer.

As noted above, in Applicant's invention (e.g., as defined in Claim 1), the semiconductor device includes a plurality of wires formed in the multi-layered insulation

film, the multi-layered insulation film being disposed between the wires. The "interlayer insulation films containing copper wires, connected to each other by interlayer connection plugs." (See Page 21, lines 1-21; and Figures 1 and 4). In addition, the semiconductor device includes a second insulation layer, which includes a polysiloxane compound having an Si-H group, formed on and adhering to a top of the first insulation layer. The invention (e.g., as recited in claim 39) also includes a second insulation layer comprised of methylated hydrogen silisesquioxane, which the Examiner acknowledges is not taught by Jeng. (See Office Action at Page 5, Section 12).

In contrast, as shown in Figures 1-3e of Jeng, Jeng merely discloses a structure, and a related method, for reducing capacitance between closely spaced interconnect lines of integrated circuits. The method improves "adhesion between low dielectric constant materials and traditional intermetal dielectric materials and protecting the low dielectric materials from subsequent processes." Jeng discloses "low-k material is deposited between interconnect lines on a semiconductor substrate", not a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires, as in the claimed invention. (See Column 3, lines 51-62).

In addition, an adhesion/protection layer covers a low k material and a dielectric layer not a a second insulation layer, which includes a polysiloxane compound having an Si-H group, formed on and adhered to a top of the first insulation layer as disclosed in Applicant's invention. Further, the adhesion layer/protection, "serves to protect the low-k polymer material from the harsh plasma CVD SiO_2 deposition environment." The adhesion layer is preferably hydrogen silisesquioxane, an inorganic dielectric. However, the adhesion/protection layer does not teach or suggest being an insulation layer as disclosed in

Applicant's invention. (See Jeng at Abstract; Column 1, lines 35-45; Column 3, lines 55-62; and Column 4, lines 43-53). Jeng has at least two significant structural differences when compared to the structure of Applicant's invention

Consequently, Jeng's conventional structure, and related method, is unsuitable for achieving at least one object of the invention, which includes providing excellent interlayer adhesion to the first insulation layer as well as with the third insulation layer while having insulative characteristics. Accordingly, the interfacial adhesion is improved between the film with low dielectric constant, i.e., the first insulation layer, and protective film, i.e., the second insulation, adhesive layer, is significantly improved, "without damaging the excellent dielectric, flatness and gap-filling characteristics of the organic material of the low dielectric constant." (See Page 6, lines 15-20; Page 16, lines 14-21).

Jeng, therefore, does not teach, suggest or disclose either a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires, or a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of the first insulation layer. (See Page 16, lines 8-21; Page 22, lines 4-6; Page 23, lines 10-15; and Figures 1-3).

For at least the reasons outlined above, Applicant respectfully submits that Jeng does not disclose, teach or suggest all the features of independent claims 1, 5 , 41 and 42. Accordingly, Jeng does not anticipate or render obvious the subject matter of claims 1, 5, 41 and 42. Withdrawal of the rejection of claims 1, 3-5, 7, 8, 34, 35, 37, 41 and 42 under 35 U.S.C. § 102(e) as anticipated by Jeng is respectfully requested.

Finally, for the above cited reasons, regarding the dependent claims 3, 4, 7, 8, 34, 35, and 37, which depend from claims 1, 5, 41 and 42, respectively, these claims are patentable

not only by virtue of their dependency from their respective independent claim but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited reference.

B. The § 103(a) Rejection Based on Jeng in view of the Admitted Prior Art

First, the references, separately, or in combination, fail to teach, disclose or provide a reason or motivation for being combined. In particular, Jeng pertains to a structure, and a related method, which integrates polymer and other low dielectric constant materials into integrated circuit substrates. Jeng is specifically directed to reducing capacitance between closely spaced interconnect lines of integrated circuits. Indeed, Jeng attempts to improve, "adhesion between low dielectric constant materials and traditional intermetal dielectric materials and protecting the low dielectric materials from subsequent processes." (See Jeng at Abstract; Column 1, lines 35-45; and Column 2, lines 38-53).

By contrast, the Admitted Prior Art ("APA") does not have the same aim as Jeng.

APA discloses a process of forming a damascene copper wiring system of a low dielectric constant material. The APA is specifically directed to decreasing inter-wire capacity in order to cope with the higher-speed operation of semiconductor devices. (See Application, Background Section, Page 1, 2nd and 3rd Paragraphs, lines 8-15).

Nothing within APA, which focuses on decreasing the inter-wire capacity in order to cope with the higher-speed operation of semiconductor devices, has anything to do with interlayer adhesion as disclosed in the Jeng. Thus, Jeng teaches away from being combined with another invention such as, for example, the APA.

Therefore, one of ordinary skill in the art would not have combined these references,

absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield Jeng and the Admitted Prior Art. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to use an alkyl silisesquioxane as taught by the prior art in the interconnect structure of Jeng to decrease inter-wire capacity. Such an assertion does not take into account the distinct structural differences and related method of Jeng as indicated above, and further discussed below. Thus, the Examiner's assertion attempts to solve a problem which does not exist with either Jeng or the APA, and this assertion is further proof of the Examiner's use of impermissible hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 1, and related claims 5, 41 and 42. Specifically, there is no teaching or suggestion of either a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires or a second insulation layer comprising a polysiloxane compound having an Si-H group, is formed on and adhering to a top of the first insulation layer.

The Examiner admits Jeng, as indicated above, also does not teach or suggest other features of independent claim 1, including a first insulation layer comprises an alkyl silisesquioxane having a dielectric of no greater than 3.5 and the wiring layer comprises copper. (See Office Action at Page 4, Section 11).

Further, APA, as indicated above, discloses a process of forming a damascene copper wiring system of a low dielectric constant material to decrease inter-wire capacity in order to cope with the higher-speed operation of semiconductor devices. Indeed, APA includes a polycrystalline silicon film formed to fill the contact hole not a plurality of wires formed in

the multi-layered insulation film as disclosed in Applicant's invention. (See Application, Page 5, lines 4-8; and Figure 9).

APA further includes a first layer composed of an organic material of low dielectric, i.e., an organic SOG film e.g., methyl silisesquioxane ("MSQ") coated with a second layer composed of an inorganic film, e.g., silicon oxide film, where the second layer is not an insulation, adhesive film as disclosed in Applicant's invention. (See Page 2, lines 12-27; and Page 6, lines 23 - Page 2, line 4).

Applicant's invention, however, is a semiconductor device, which includes a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires. Further, the second insulation layer includes a polysiloxane compound having an Si-H group and formed on and adhering to a top of the first insulation layer. The second layer provides excellent interlayer adhesion to the first insulation layer as well as with the third insulation layer while having insulative characteristics. Accordingly, the interfacial adhesion is improved between the film with low dielectric constant, i.e., the first insulation layer, and protective film, i.e., the second insulation layer, is significantly improved, "without damaging the excellent dielectric, flatness and gap-filling characteristics of the organic material of the low dielectric constant." (See Page 6, lines 15-20; Page 16, lines 14-21). Thus, Applicant's invention does not teach or suggest forming a damascene copper wiring system of a low dielectric constant material to decrease inter-wire capacity in order to cope with the higher-speed operation of semiconductor devices as with Jeng. Thus, Jeng, as discussed above, does not disclose, teach or suggest Applicant's invention. The admitted prior art does not make up for the deficiencies of Jeng.

For at least the reasons outlined above, Applicant respectfully submits that Jeng in

view of the Admitted Prior Art does not teach or suggest all the features of independent claims 1 and 5, and related dependent claims 2, 6, 31-33 and 38.

Regarding the dependent claims 2, 6, 31-33 and 38, which depend from claims 1 and 5, these claims are patentable not only by virtue of their dependency from their respective independent claims but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

C. The § 103(a) Rejection Based on Jeng in view of Allada

Allada, et al. ("Allada") does not have the same aim as Jeng.

Allada pertains to multilevel interconnects for integrated circuit devices, in particular, copper/dual damascene devices, and related fabrication methods. "Methylated-oxide type hardmasks are formed over polymeric interlayer dielectric materials" where the hardmask and the interlayer dielectric may be spincoated. The interconnect integration eliminates "the need for removal of the wafer after formation of a polymeric interlayer dielectric to equipment for forming conventional oxide hardmasks on interlayer dielectrics. This invention increases device speed by reducing the effective dielectric constant in the stack, and the structures created thereby. (See Allada at Abstract; Column 1, lines 7-12; and Column 2, lines 5-25). Accordingly, Allada has a different focus than Jeng which, as discussed above, is a low capacitance interconnect structure, and method, for integrating polymers and other low dielectric constant materials into integrated circuit substrates to improve, "adhesion between low dielectric constant materials and traditional intermetal dielectric materials and protecting the low dielectric materials from subsequent processes." (See Jeng at Abstract; Column 1, lines 35-45; and Column 2, lines 38-53).

Therefore, one of ordinary skill in the art would not have combined Jeng and Allada to form the claimed invention, absent hindsight. It is clear that Applicant's specification was simply read and a keyword search conducted to yield Jeng and Allada. Further, the Examiner provides no motivation or reason to assert that it would have been obvious to one having ordinary skill in the art at the time to "use the insulating layer as taught by Allada et al. in the interconnect formation structure of Jeng, since this dielectric layers exhibit low dielectric constants." Such an assertion does not take into account the distinct structural and related method differences of the inventions as indicated above. Thus, this assertion attempts to solve a problem which does not exist with either Jeng or Allada.

Second, even if combined, Allada like Jeng also does not disclose, teach or suggest the features of independent claim 1, including a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires or a second insulation layer comprising a polysiloxane compound having an Si-H group, is formed on and adhering to a top of the first insulation layer.

Rather, Allada discloses a conventional multilevel interconnect for integrated circuit devices for copper/dual damascene devices, and related fabrication methods where "methylated-oxide type hardmasks are formed over polymeric interlayer dielectric materials." (See Allada at Abstract; Column 1, lines 7-12; and Column 2, lines 5-25). Allada disclose a alternating layers of hardmasks with a specific dielectric and polymer dielectrics whereas Applicant discloses a plurality of wires formed in the multi-layered insulation film, the multi-layered insulation film being disposed between the wires.

Further, in Allada, none of the four alternating layers of polymeric interlayer dielectric and hardmask explicitly has both insulative and adhesive properties as in the second

insulation, adhesive layer of Applicant's invention. (See Column 3, lines 14-20). Indeed, Allada has a different function as the hardmask is not used as an adhesive but merely as a mask. Here, the hardmask is between two polymer layers not between a polymer layer and SiO_2. Therefore, there is no adhesive function. (See Column 3, lines 5-20).

Finally, Applicant traverses the assertion that Figures 1a-1b of Allada teach a second insulation film comprising a methylated hydrogen silsesquioxane as Allada only teaches methylated oxide -type dielectrics. Allada certainly does not teach or suggest any polysiloxane compound, let alone, "methylated hydrido organo siloxane polymer" as incorrectly suggested in the Office Action. (See Allada, Column 2, lines 7-58; Office Action at Page 5, Section 12).

For at least the reasons outlined above, Applicant respectfully submits that Jeng in view of Allada fails to teach or suggest all of the features of independent claim 1, and related dependent claims 39 and 40.

Regarding dependent claims 39 and 40, which depend from claim 1, these claims are patentable not only by virtue of their dependency from the respective independent claim, but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-8 and 31-42, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above

application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 1/30/03

Fredric J. Zimmerman, Esq.
Reg. No. 48,747

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

The following claims have been amended:

1. (Amended) A semiconductor device comprising:

a multi-layered insulation film formed on a semiconductor substrate, said multi-layered insulation film comprising:

a first insulation layer comprising an organic material having a dielectric constant which is lower than a silicon oxide dielectric constant;

a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of said first insulation layer; [and]

a third insulation layer comprising an inorganic material and formed on and adhering to a top of said second insulation layer[.]; and

a plurality of wires formed in said multi-layered insulation film, said multi-layered insulation film being disposed between said wires.

5. (Amended) A semiconductor wafer comprising:

a multi-layered insulation film formed on a surface of the wafer, said multi-layered insulation film comprising:

a first insulation layer comprising an organic material having a dielectric constant which is lower than a silicon oxide dielectric constant;

a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of said first insulation layer; [and]

a third insulation layer comprising an inorganic material and formed on and

adhering to a top of said second insulation[.], and

a plurality of wires formed in said multi-layered insulation film, said multi-layered insulation film being disposed between said wires.

36. (Amended) The semiconductor device according to claim [36] 1, wherein said second insulation layer comprises methyl silisesquioxane.

41. (Amended) A semiconductor device having a damascene wiring structure, said semiconductor device comprising:

a multi-layered insulation film formed on a semiconductor substrate, said multi-layered insulation film having a plurality of recesses and comprising:

a first insulation layer comprising an organic material having a dielectric constant which is lower than a silicon oxide dielectric constant;

a second insulation layer comprising a polysiloxane compound having an Si-H group and formed on and adhering to a top of said first insulation layer;

a third insulation layer comprising an inorganic material and formed on and adhering to a top of said second insulation layer; and

an electroconductive film formed in each recess in said plurality of recesses[.],

said multi-layered insulation film being disposed between each recess having said electroconductive film.

42. (Amended) A semiconductor device comprising a multi-layered insulation film and a plurality of wires formed on a semiconductor substrate said multi-layered insulation film

comprising:

a first insulation layer comprising an organic material having a dielectric constant which is lower than a silicon dioxide dielectric constant;

a second insulation, adhesive layer comprising a polysiloxane compound having an Si-H group and formed on and being in contact with a top of said first insulation layer; and

a third insulation layer comprising an inorganic material and formed on and being in contact with a top of said second insulation, adhesive layer[.],

wherein said multi-layered insulation film is disposed between said wires in said plurality of wires.